IN THE CLAIMS:

1. A multilayer semiconductor device assembly jig, comprising:

a lateral position restriction mechanism for positioning a plurality of stacked semiconductor modules on a base member with their respective lateral positions mutually restricted;

a height restriction mechanism for restricting an entire height of said semiconductor modules layered on said base member; and

an alignment mechanism for providing alignment with reference to a mother substrate; and further wherein a plurality of the semiconductor modules are each comprised of a single semiconductor chip secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein a plurality of adjacent printed wiring board members are secured to one another by solder connections between top and bottom surfaces thereof.

2. (Not Modified) The multilayer semiconductor device assembly jig according to claim 1 comprising a box-shaped member which is positioned on said base member and having a storage space for storing said semiconductor modules in a layered state,

wherein an inner wall of said storage space constitutes said lateral position restriction mechanism.

3. (Not Modified) The multilayer semiconductor device assembly jig according to claim 2, wherein said alignment mechanism comprises a plurality of positioning pins and positioning holes for receiving the positioning pins which are correspondingly formed in said box-shaped member and said mother substrate.

4. (Not Modified) The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins secured in said base member and which are used for securing at least three different portions of an outer periphery of said semiconductor modules.

5. (Amended) The multilayer semiconductor device assembly jig according to claim 1, wherein said position restriction mechanism further comprises a plurality of positioning pins ~~provided~~ secured in said base member and which pierce through positioning holes formed in said semiconductor modules.

6. (Not Modified) The multilayer semiconductor device assembly jig according to claim 5, wherein said positioning pins also pierce through a positioning hole formed on said mother substrate.

7. (Not Modified) The multilayer semiconductor device assembly jig according to claim 1, wherein said height restriction mechanism further comprises:

a cover member secured over said semiconductor modules.

8. (Amended) A multilayer semiconductor device manufacturing method using an assembly jig for mutually restricting positions of a plurality of semiconductor modules each including a semiconductor chip mounted on a thin printed-wiring board comprising the steps of:

serially layering the semiconductor modules on a base member with respective lateral positions restricted by a lateral position restriction mechanism and placing said assembly jig with an entire height of said layered modules restricted by said height restriction mechanism,

supplying said assembly jig into a reflow furnace, applying reflow heating to melt solder bumps and for thereby forming interlayer connection among said semiconductor modules, and thus forming a layered semiconductor module unit; and

mounting said layered semiconductor module unit on a mother substrate by using a top-layer semiconductor module as a junction module <u>and further wherein a plurality of the semiconductor modules are each comprised of a single semiconductor chip secured to a printed wiring board that has electrical connections on a top and bottom surface thereof and wherein a plurality of adjacent printed wiring board members are secured to one another by solder connections between top and bottom surfaces thereof</u>.

9. (Not Modified) The multilayer semiconductor device manufacturing method according to claim 8, further comprising a step of providing said assembly jig with an alignment mechanism for aligning said layered semiconductor module unit against said mother substrate.

10. (Not Modified) The multilayer semiconductor device manufacturing method according to claim 8 further comprising the step of:

forming a bump on each of connection lands and dummy lands of printed wiring board for each semiconductor module.